
Fact Sheet

ALTIVEC™ TECHNOLOGY

MOTOROLA'S HIGH-PERFORMANCE VECTOR PARALLEL PROCESSING EXPANSION TO THE POWERPC ARCHITECTURE™

Motorola's new AltiVec technology expands the capabilities of PowerPC™ microprocessors by providing leading-edge, general-purpose processing performance while concurrently addressing high-bandwidth data processing and algorithmic-intensive computations in a single-chip solution.

Traditionally, many high-performance applications have contained a combination of a single microprocessor performing the system control function and off-chip devices based on one or more other architectures, such as a DSP farm or custom ASICs, to perform specialized computations. AltiVec technology will enable a new class of processors that provides for the convergence of these technologies. AltiVec technology provides embedded and computing system designers with a new "one part—one code base" approach to product design. Because this integrated solution is still 100% compatible with the industry standard PowerPC architecture, design and support are simplified and the development barriers inherent to multiple architecture designs are eliminated. System designers and their customers will benefit through the reduced time-to-market and lowered total system development expense while simultaneously enjoying a tremendous jump in performance.



New Execution Unit & New Instructions Provide New Capabilities

Motorola's AltiVec technology expands the current PowerPC architecture through the addition of a 128-bit vector execution unit, which operates concurrently with the existing integer and floating point units. This new engine provides for highly parallel operations, allowing for the simultaneous execution of up to 16 operations in a single clock cycle.

AltiVec technology is a short vector parallel architecture. Depending on data size, vectors are 4, 8 or 16 elements long. This can be contrasted with the long vector architectures of supercomputers that were popular in the 1980s. Vector sizes for those machines ranged to hundreds of elements. The long vector approach of supercomputers, while useful for scientific calculations, is not optimal for the communications, multimedia and other performance-driven applications targeted by Motorola with AltiVec technology.

AltiVec technology operations are performed on multiple data elements by a single instruction. This is often referred to as SIMD (single instructions, multiple data) parallel processing. AltiVec technology offers support for:

- 16-way parallelism for 8-bit signed and unsigned integers and characters
- 8-way parallelism for 16-bit signed and unsigned integers
- 4-way parallelism for 32-bit signed and unsigned integers and IEEE floating-point numbers

AltiVec technology also includes a separate register file containing 32-entries, each 128-bits wide. These 128-bit wide registers hold the data sources for the AltiVec technology execution units. Registers are loaded and unloaded through vector store and vector load instructions that transfer the contents of a single 128-bit register to and from memory.

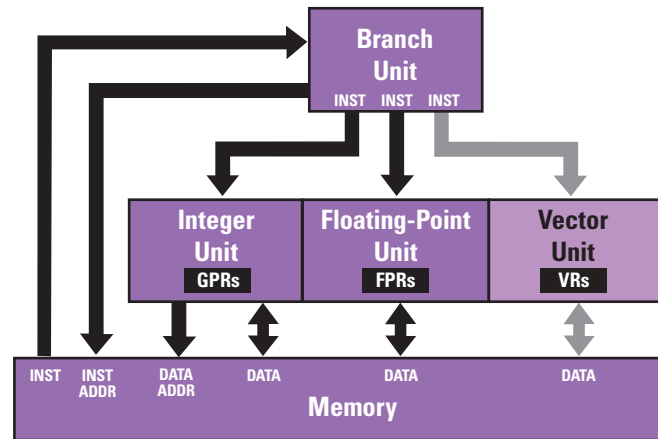
AltiVec technology can be most accurately thought of as a set of registers and execution units added to the PowerPC architecture in an analogous manner to the addition of floating point units. Floating point units were added to most mainstream microprocessor architectures to provide better support for high-precision

scientific calculations. AltiVec technology is being added to the PowerPC architecture to dramatically accelerate the next level of performance-driven, high-bandwidth communications and computing applications.

Each AltiVec instruction specifies up to three source operands and a single destination operand. All operands are vector registers, with the exception of the load and store instructions and a few instruction types that provide operands from immediate fields within the instruction. 162 new unique instructions are defined for the AltiVec technology. These instructions fall into the following major classes:

- Intra-element arithmetic operations
- Intra-element non-arithmetic operations
- Inter-element arithmetic operations
- Inter-element non-arithmetic operations

High-level structural overview for PowerPC with AltiVec technology



Applications of AltiVec Technology

The initial target applications for PowerPC processors utilizing AltiVec technology include:

- IP telephony gateways
- Speech processing systems
- Image and video processing systems
- Internet routers
- Multi-channel modems,
- Echo cancelers
- Scientific array processing systems
- Virtual private network servers.

In addition to accelerating next-generation applications, AltiVec technology can, through its wide datapaths and wide field operations, also accelerate many time-consuming traditional computing and embedded processing operations such as memory copies, string compares and page clears.

Unlike fixed function solutions which are most often implemented as application specific integrated circuits, AltiVec technology will offer a programmable solution that can easily migrate via software upgrades to follow changing standards and customer requirements. The preferred programming environment is the C and C++ languages favored by embedded systems developers. Motorola is working with leading tools providers to develop simulators, assemblers, linkers and compilers to assure full support for the AltiVec technology.

While the initial PowerPC microprocessor utilizing AltiVec technology will target very high-performance applications in networking and computing applications, subsequent Motorola processors with AltiVec technology could address markets and applications in which performance must be balanced with power, price and peripheral integration.

Contact Information

- For more information on AltiVec technology, including programming models and white papers, visit Motorola's AltiVec Technology website at:

<http://motorola.com/AltiVec/>

- For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at:

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